LM64P839
Passive Matrix LCD Unit

FEATURES

- Display Format: 640 × 480
- Overall Dimensions:
  253 (W) × 174 (H) × 7 (D) mm
- Active Area: 196 (W) × 147.6 (H) mm
- Dot Pitch: 0.27 (W) × 0.27 (H) mm
- Response/Contrast Ratio: 150 ms/18:1
- Viewing Mode: Transmissive

DESCRIPTION

The SHARP LM64P839 is a 640 × 480 dot display unit consisting of an LCD panel, Printed Wiring Board (PWB) with electric components mounted on it, Tape Automated Bonding (TAB) to connect the LCD panel and PWB electrically, and a plastic chassis with a CCFT backlight and bezel to fit them mechanically.

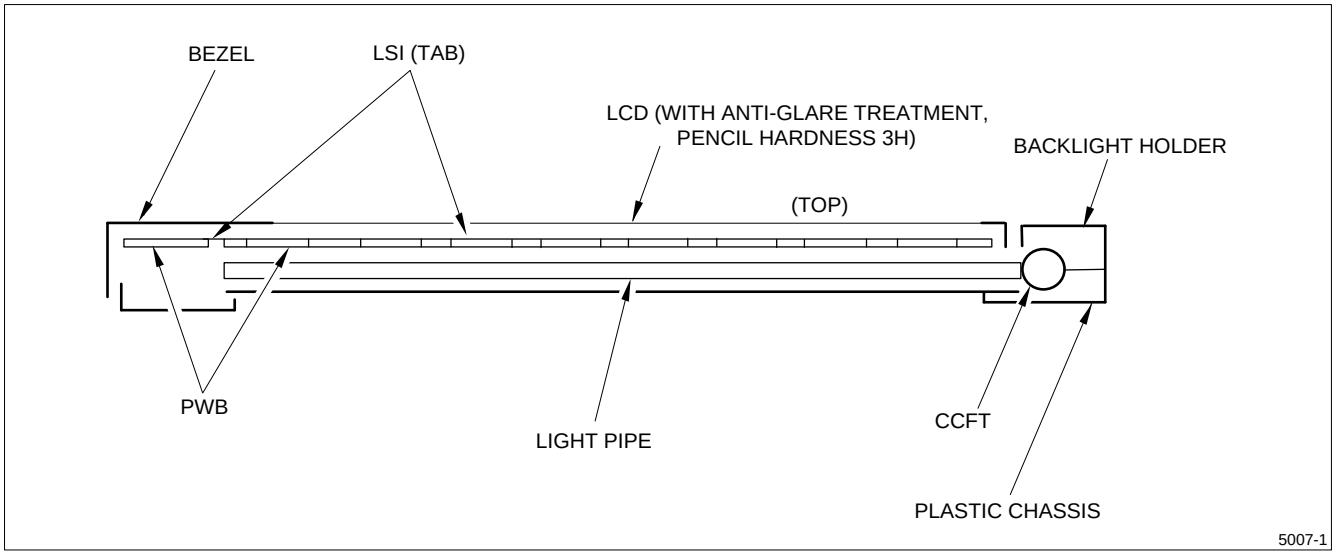


Figure 1. LM64P839 Construction

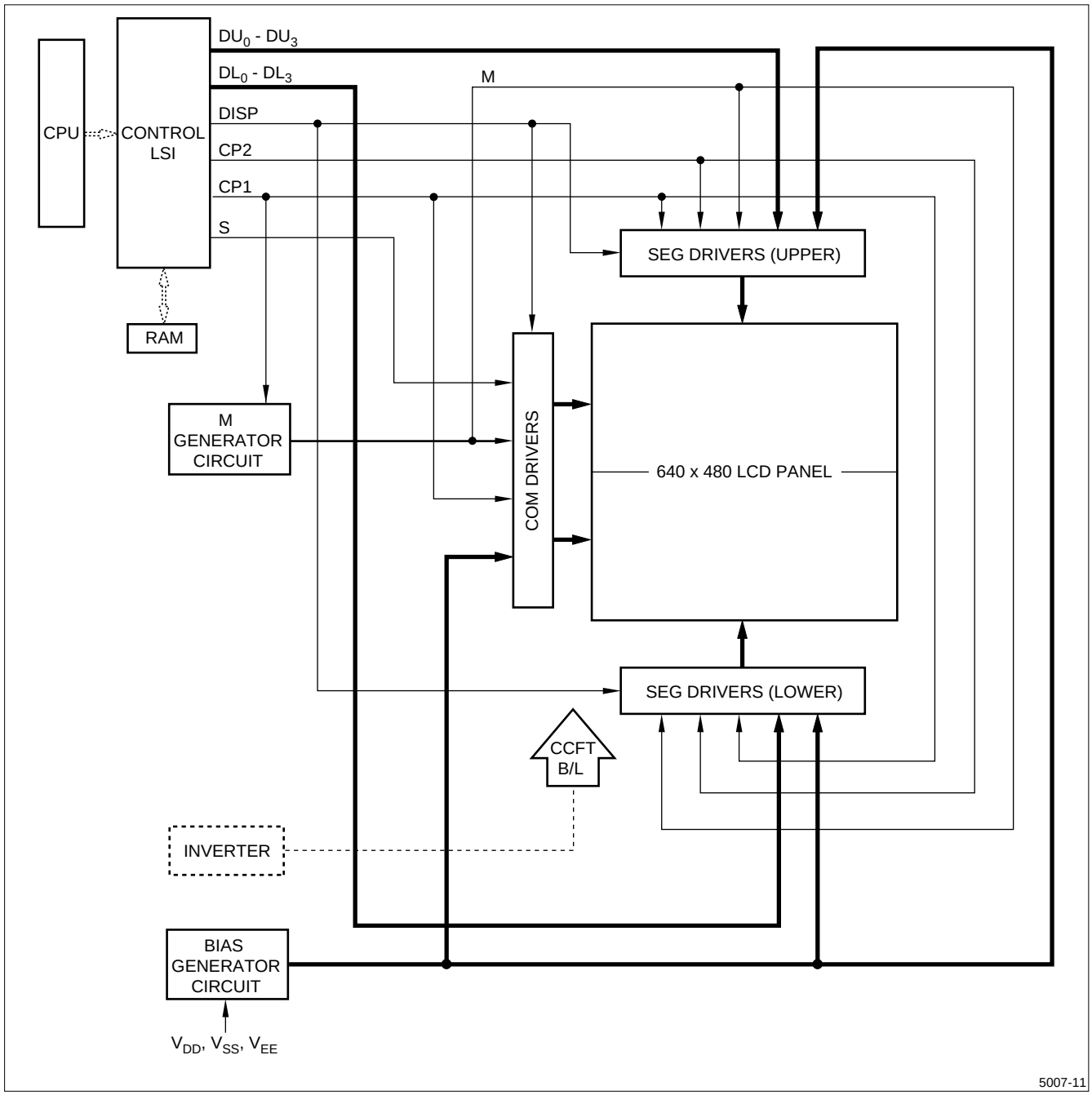


Figure 2. LM64P839 Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT	NOTE
Outline Dimensions	253 (W) × 174 (H) × 7 max (D)	mm	1
Active Area	196 (W) × 147.6 (H)	mm	–
Display Format	640 (W) × 480 (H) Full Dot	–	–
Dot Size	0.27 × 0.27	mm	–
Dot Spacing	0.03	mm	–
Dot Color	White	–	2, 3
Background Color	Black	–	2, 3
Weight	Approximately 340	g	–

NOTES:

1. Excludes the mounting tabs.
2. Due to the characteristics of the LC material, the colors vary with environmental temperature.
3. Negative-type display:
   Displayed data 'H': Dots ON: White
   Displayed data 'L': Dots OFF: Black

ABSOLUTE MAXIMUM RATINGS (t_A = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD} – V_{SS}$	Supply Voltage (Logic)	0	6.0	V
$V_{DD} – V_{EE}$	Supply Voltage (LCD Drive)	0	30.0	V
V_{IN}	Input Voltage	0	V_{DD}	V

ENVIRONMENTAL CONDITIONS

ITEM	Tstg		Topr		CONDITION	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	–25°C	+60°C	0°C	+45°C	–	1
Humidity	–		–		No condensation	2
Vibration	–		–		3 Directions (X/Y/Z)	3
Shock	–		–		6 Directions (±X/±Y/±Z)	4

NOTES:

1. Do not subject the LCD unit to temperatures out of this specification.
2. $t_A \leq 40°C$, 95% RH maximum.
   $t_A > 40°C$, Absolute humidity less than $t_A = 40°C$ at 95% RH.
3. These test conditions are in accordance with 'IEC 68-2-66' as shown in the following table (two hours for each direction of X/Y/Z (six hours total)):

Frequency	10 Hz to 57 Hz	57 Hz to 500 Hz
Vibration Level	–	9.8 m/s^2 (1 G)
Vibration Width	1 mm	–
Interval	10 Hz to 500 Hz to 10 Hz/11 minimum	

4. Acceleration: 490 m/s^2 (50 G)
   Pulse width: 11 ms
   Three times for each direction of ±X/±Y/±Z

ELECTRICAL CHARACTERISTICS (t_A = 25°C, V_{DD} = 5.0 V ±5%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
$V_{DD} – V_{SS}$	Supply Voltage (Logic)	–	4.75	5.0	5.25	V	–
$V_{EE} – V_{SS}$	Supply Voltage (LCD Drive)	–	–23.2	–18.9	–15.1	V	1, 2
V_{IN}	Input Signal Voltage	'H' Level	0.8 V_{DD}	–	V_{DD}	V	–
		'L' Level	0	–	0.2 V_{DD}	V	–
I_{IL}	Input Leakage Current	'H' Level	–	–	250	µA	–
		'L' Level	–250	–	–	µA	–
I_{DD}	Supply Current (Logic)	–	–	24	36	mA	3
I_{EE}	Supply Current (LCD Drive)	–	–	15	25	mA	
P_D	Power Consumption	–	–	410	660	mW	

NOTES:

1. The viewing angle **θ** at which the optimum contrast is obtained can be set by adjusting $V_{EE} – V_{SS}$. Refer to Figure 7 for the definition of viewing angle **θ**.
2. Maximum and minimum values are specified as the maximum and minimum voltage within the operating temperature range (0°C to 45°C). Typical values are specified as the typical voltage at 25°C.
3. Display high frequency pattern: V_{DD} = 5 V, $V_{EE} – V_{SS}$ = –18.9 V, frame frequency = 85 Hz, display pattern = 1-bit checker (Figure 3).

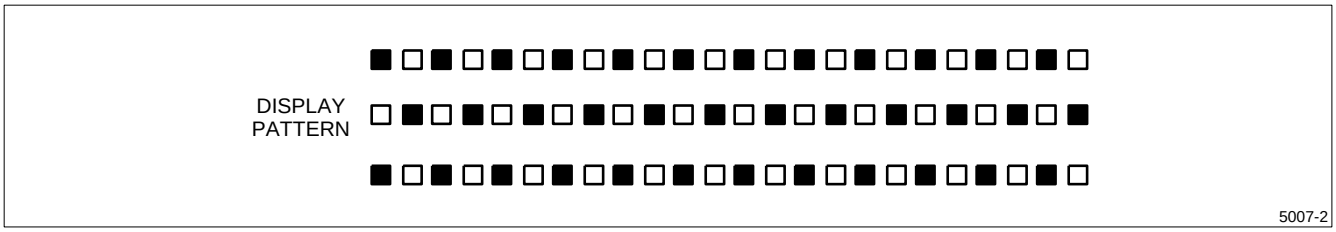


Figure 3. Display High Frequency Pattern

INPUT CAPACITANCE

SIGNAL	INPUT CAPACITANCE (TYPICAL)
S	40 pF
CPI, DISP	250 pF
CP2	200 pF
$DU_0 – DU_3$	200 pF
$DL_0 – DL_3$	200 pF

INTERFACE SIGNALS

LCD [1]

PIN NUMBER [2]	SYMBOL	DESCRIPTION	LEVEL
1	S	Scan Start-Up Signal	'H'
2	CP1	Input Data Latch Signal	H → L
3	CP2	Data Input Clock Signal	H → L
4	DISP	Display Control Signal	Display on . . . 'H' Display off . . . 'L'
5	V_{DD}	Power Supply for Logic and LCD (+5 V)	–
6	V_{SS}	Ground Potential	–
7	V_{EE}	Power Supply for LCD (–)	–
8	DU_0	Display Data Signal (Upper Half)	H (ON), L (OFF)
9	DU_1		
10	DU_2		
11	DU_3		
12	DL_0	Display Data Signal (Lower Half)	H (ON), L (OFF)
13	DL_1		
14	DL_2		
15	DL_3		

NOTES:

1. Connector used: 53261-1510 (MOLEX)
   Mating connector: 51021-1500 (MOLEX)
2. Pin Number and its location are shown in the Outline Dimension diagram.

CCFT [1]

PIN NUMBER [2]	SYMBOL	DESCRIPTION	LEVEL
1	GND	Ground Line (From Inverter)	–
2	NC	–	–
3	NC	–	–
4	HV	High Voltage Line (From Inverter)	–

NOTES:

1. Connector used: M63M83-04 (MITSUMI)
   Mating connector: M60-04-30-114P (MITSUMI), M60-04-30-134P (MITSUMI), M61M73-04 (MITSUMI)
2. Pin Number and its location are shown in the Outline Dimensions diagram.

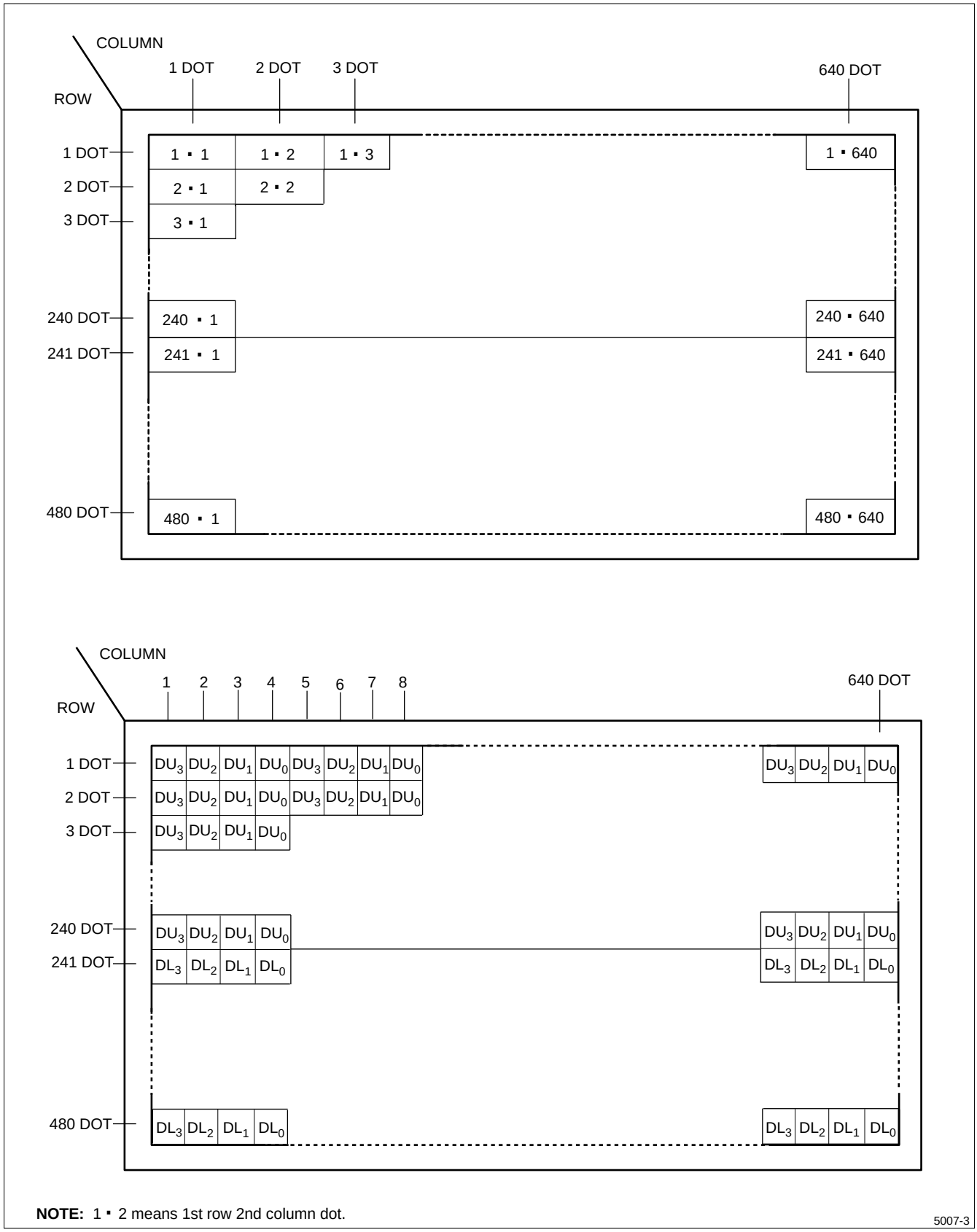


Figure 4. Dot Chart of Display Area

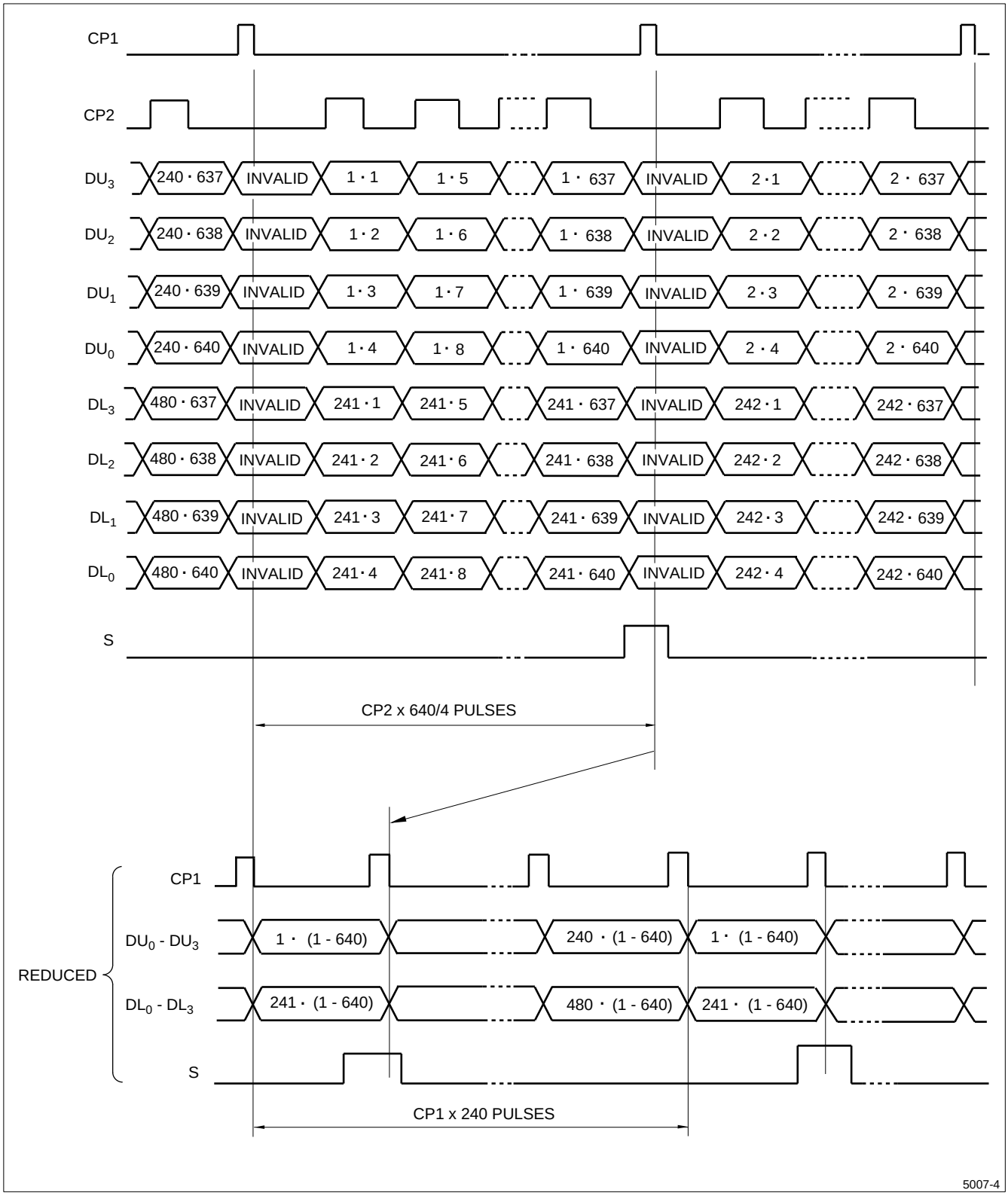
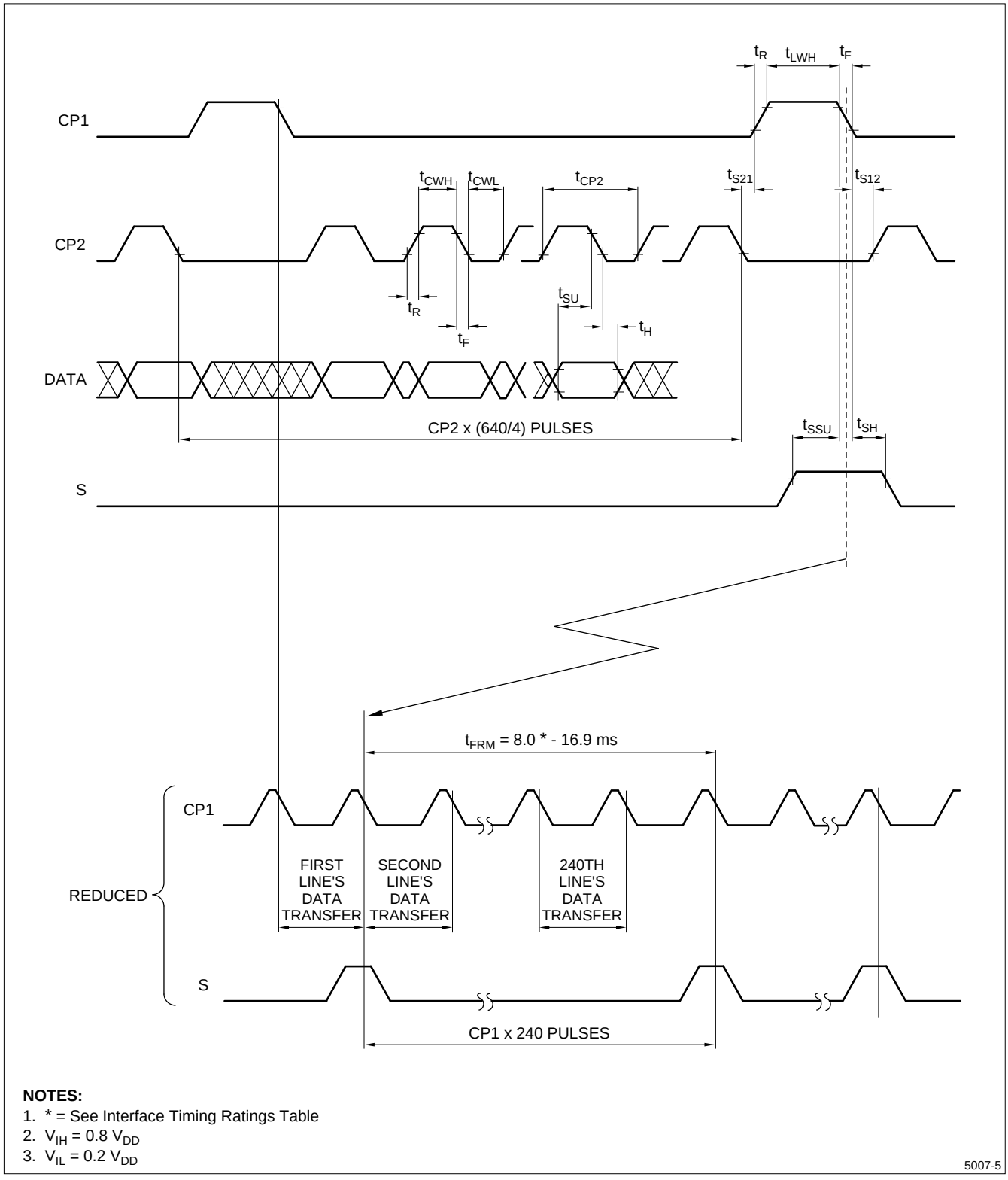


Figure 5. Data Input Timing



NOTES:
1. * = See Interface Timing Ratings Table
2. $V_{IH} = 0.8\ V_{DD}$
3. $V_{IL} = 0.2\ V_{DD}$

Figure 6. Interface Timing Chart

INTERFACE TIMING RATINGS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
t_{FRM}	Frame Cycle	8.0	–	16.9	ms	1
t_{CP2}	CP2 Clock Cycle	152	–	–	ns	–
t_{CWH}	'H' Level Clock Width	65	–	–	ns	–
t_{CWL}	'L' Level Clock Width	65	–	–	ns	–
t_{LWH}	'H' Level Latch Clock Width	70	–	–	ns	–
t_{SU}	Data Setup Time	50	–	–	ns	–
t_H	Data Hold Time	40	–	–	ns	–
t_{SSU}	S Setup Time	100	–	–	ns	–
t_{SH}	S Hold Time	100	–	–	ns	–
t_{S21}	CP2 ↑ Clock Allowance Time From CP1 ↓	0	–	–	ns	–
t_{S12}	CP1 ↑ Clock Allowance Time From CP2 ↓	0	–	–	ns	–
t_R, t_F	Clock Rise/Fall Time	–	–	t_{RF}	ns	2

NOTES:

1. The LCD unit functions at the minimum frame cycle of 8 ms (maximum frame frequency of 125 Hz). Due to the characteristics of the LCD unit, 'shadowing' becomes more evident as frame frequency goes up, while flicker is reduced. According to our experiments, a minimum frame cycle of 11.7 ms or a maximum frame frequency of 85 Hz demonstrates optimum display quality in terms of flicker and 'shadowing.' Since visual judgement of display quality is subjective, and display quality such as 'shadowing' is pattern dependent, base frame cycle or frame frequency, to which power consumption of the LCD unit is proportional, on thorough testing of the LCD unit with every possible pattern displayed on it.
2. $t_{RF} = 50$ in case $t_{CT} = (t_{CP2} - t_{CWH} - t_{CWL})/2 \geq 50$
   $t_{RF} = t_{CT}$ in case $t_{CT} = (t_{CP2} - t_{CWH} - t_{CWL})/2 < 50$

UNIT DRIVING METHOD

Circuit Driving Method

Figure 2 shows the block diagram of the unit's circuitry.

Display Face Configuration

The display face electrically consists of two (upper and lower) display segments so that the unit can offer higher contrast by reducing drive duty ratio. Each display segment (640 × 240 dots) is driven at 1/240 duty ratio.

Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits, and LCD driver circuits.

Display data, which are externally divided into data for each row (640 dots), is sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of one row (640 dots) have been input, they are latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Then the corresponding drive signal is transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S is transferred from the scan signal driver to the first row of scan electrodes, and the contents of the data signals are displayed on the first rows of upper and lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the first rows of data are being displayed, the second rows of data are entered. When 640 dots of data have been transferred, then latched, on the falling edge of CP1 clock, the display face proceeds to the second rows of display.

Such data input is repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display using the time-sharing method. Then data input proceeds to the next display face.

Scan start-up signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which deteriorates LCD materials, drive waveform is inverted at every display frame by Control Signal M to prevent the generation of such DC voltage.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of transferring 4 bits parallel data through the four lines of shift registers to reduce the data transfer speed CP2. This system minimizes power consumption of the unit.

In this circuit configuration, 4-bit display data are input to data input pins of $DU_0 – DU_3$ (upper display segment) and $DL_0 – DL_3$ (lower display segment).

The LCD unit also adopts a bus line system for data input to minimize the power consumption. In this system, data input terminal of each driver LSI is activated only when relevant data input is fed.

Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

- The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20 CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.
- This process is immediately followed at the column driver's LSIs of both the upper and the lower display segments. Thus, data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no refresh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals is shown in Figure 6 and the Interface Timing Ratings table.

OPTICAL CHARACTERISTICS (t_A = 25°C, V_{DD} = 5.0 V, $V_{DD} - V_{EE} = V_{MAX}$)

The following specifications are based on the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x = \theta y = 0°$) is maximum.

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
θx	Viewing Angle Range	$C_0 > 4.0$	$\theta y = 0°$	–25	–	25	degrees	1
θy			$\theta x = 0°$	–10	–	20		
C_0	Contrast Ratio	$\theta x = \theta y = 0°$		10	18	–	–	2
t_R	Response Time – Rise	$\theta x = \theta y = 0°$		–	80	130	ms	3
t_D	Response Time – Decay	$\theta x = \theta y = 0°$		–	70	120	ms	

NOTES:

1. The viewing angle range is defined as shown in Figure 7.
2. Contrast Ratio is defined as follows:

   $$C_0 = \frac{\text{Luminance(brightness) all pixels 'white' at } V_{MAX}}{\text{Luminance (brightness) all pixels 'dark' at } V_{MAX}}$$

   V_{MAX} is defined in Figure 9.
3. The response characteristics of the photodetector output are measured as shown in Figure 10, assuming that input signals are applied to select and deselect the dots to be measured, in the optical characteristics test method shown in Figure 11.

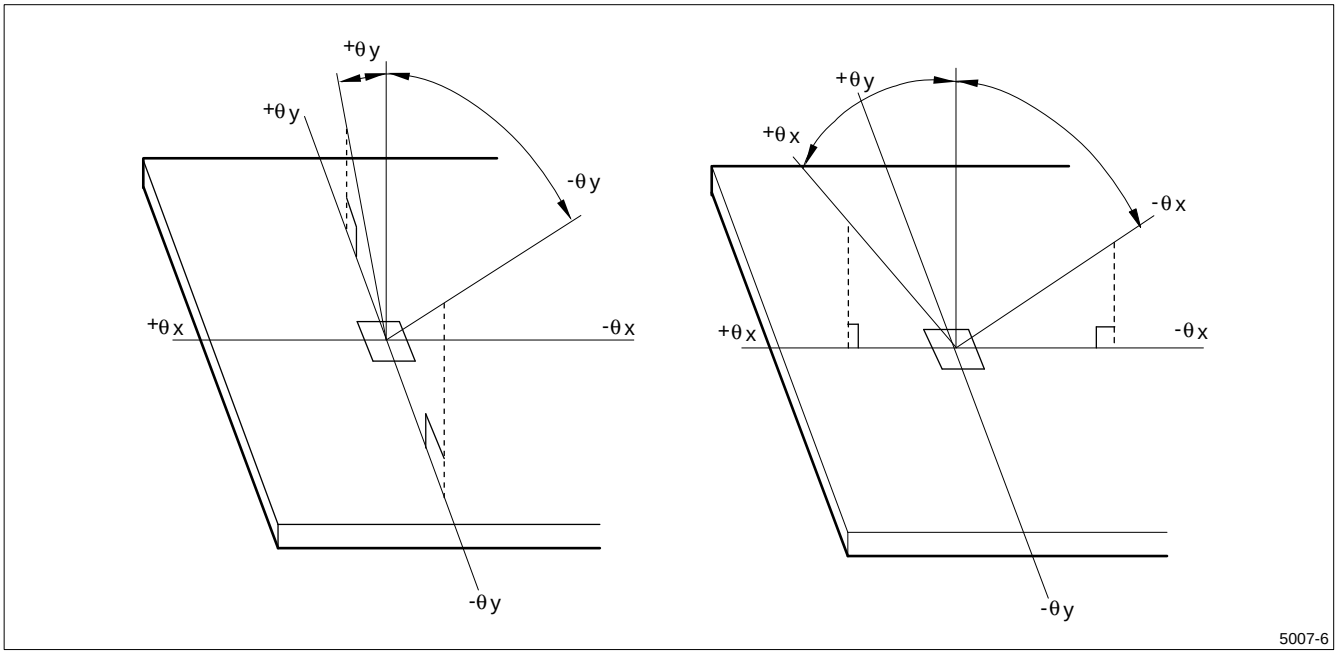
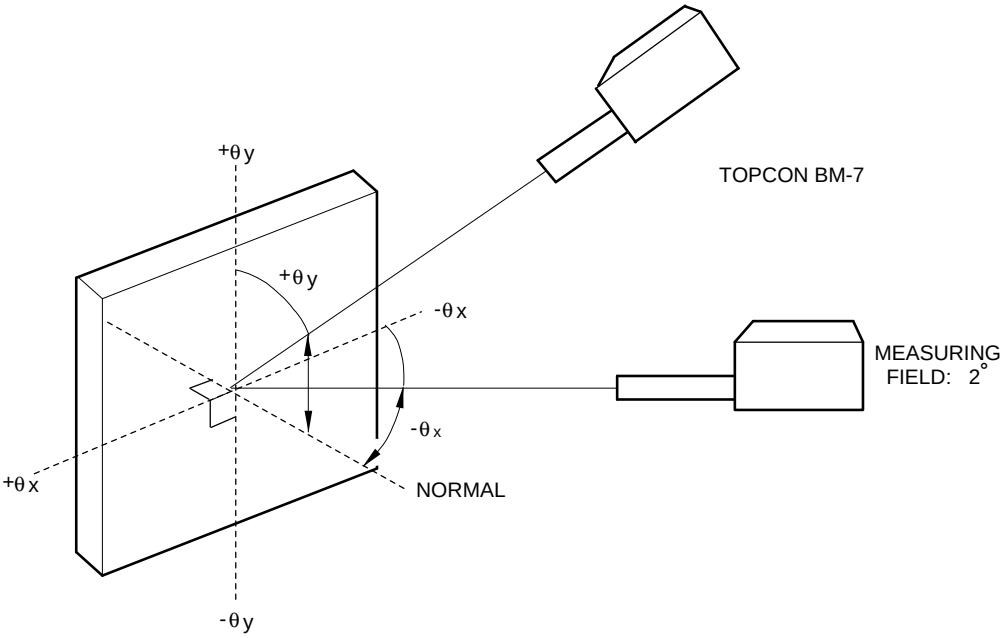


Figure 7. Definition of Viewing Angle



NOTES:
Measuring Spot Size: ϕ10 mm
θx: Angle from 'normal' to viewing surface rotated about the horizontal axis.
θy: Angle from 'normal' to viewing surface rotated about the vertical axis.

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Figure 8. Optical Characteristics Test Method I

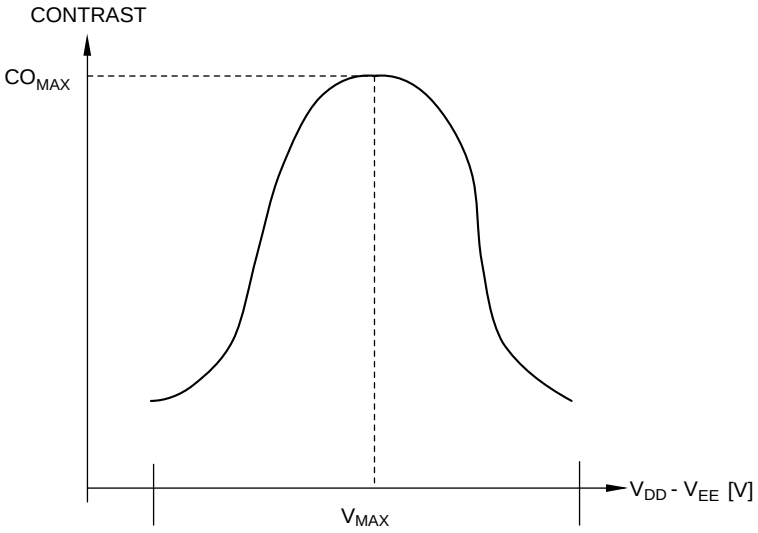

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Figure 9. Definition of V_{MAX}

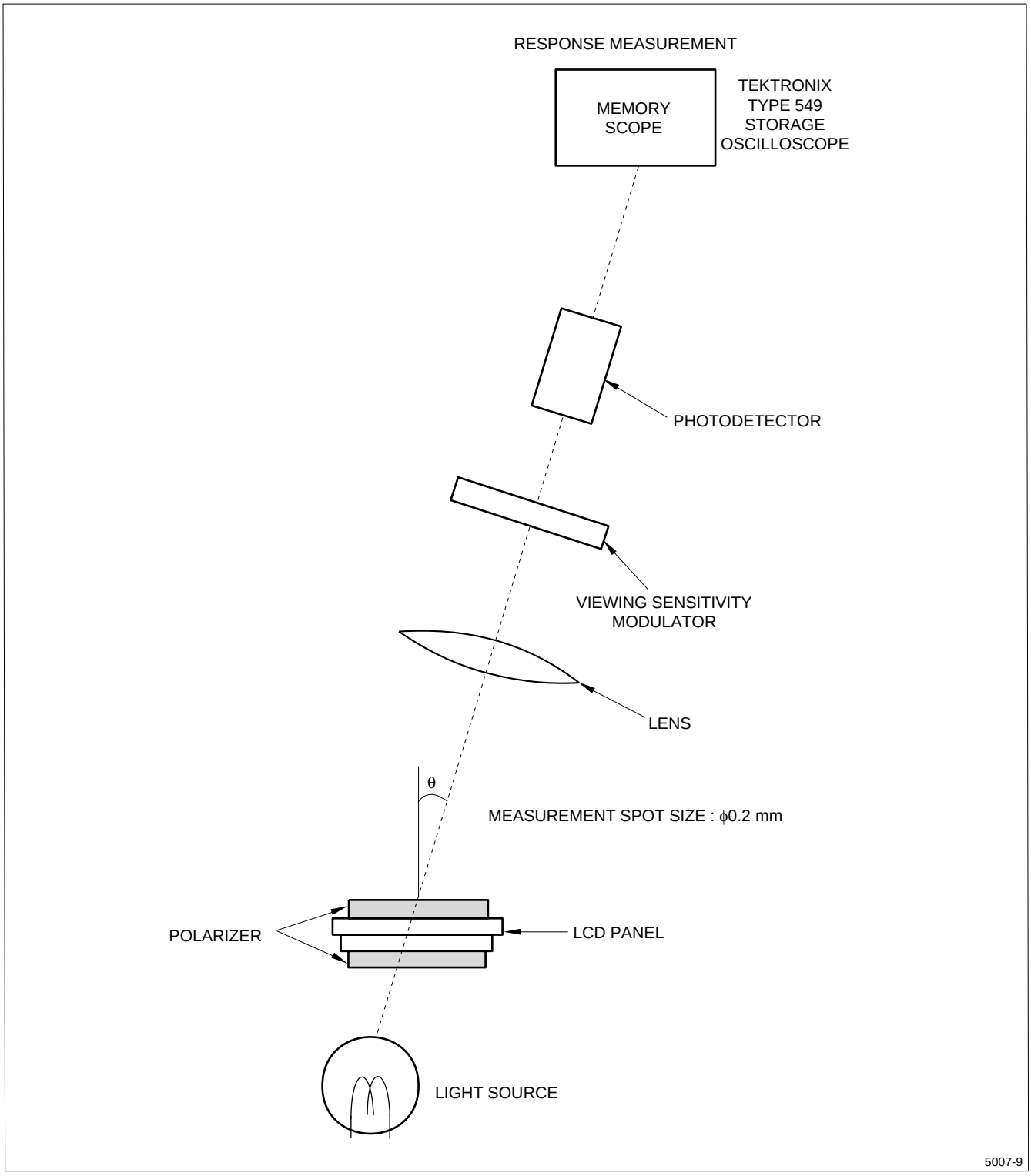


Figure 10. Optical Characteristics Test Method II

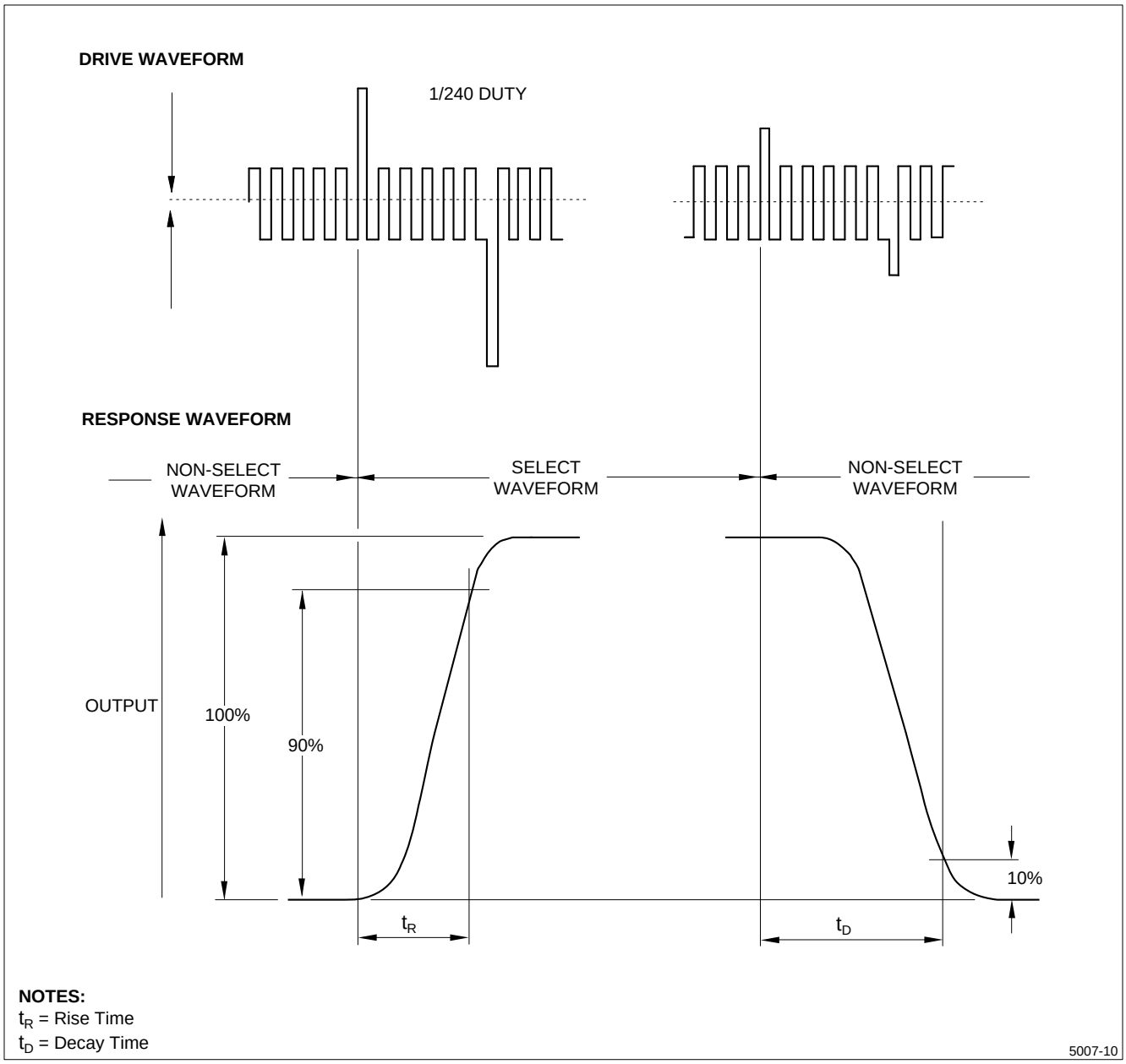


Figure 11. Definition of Response Time

CHARACTERISTICS OF BACKLIGHT

The ratings satisfy the following conditions.

Rating

PARAMETER	MIN.	TYP.	MAX.	UNIT
Brightness	40	65	–	cd/m^2

Measurement Circuit

LM000106 (SHARP) (at I_L = 5 mA RMS)

Measurement Equipment

BM-7 (TOPCON)

Measurement Conditions

- Measurement circuit voltage: DC = 12 V at primary side.
- LCD: All digits WHITE, V_{DD} = 5 V, $V_{DD} – V_{EE} = V_{MAX}$, $DU_0 – DU_3$ (refer to Figure 9), $DL_0 – DL_3$ = 'H' (WHITE)
- Ambient temperature: 25°C. Make measurement 30 minutes after turning on the unit.

Lamp Used (Ratings, 1pc.)[1]

FLE-30164C (FA) B-NS115, 1 pc.

PARAMETER		MAXIMUM ALLOWABLE VALUE	NOTE
Circuit Voltage (VS)	1,000 V_{RMS} (minimum)	1,500 V_{RMS}	–
Discharging Tube Current (IL)	5 mA_{RMS} (typical)	7 mA_{RMS}	2
Power Consumption	1.7 W	–	–
Discharging Tube Voltage (VL)	340 V_{RMS} (typical)	–	–
Brightness (B)	27,000 cd/m^2 (typical)	–	–

NOTES:

1. Within no conductor closed.
2. It is recommended that IL be not more than 5 mA_{RMS} so that heat radiation of CCFT backlight least affects the display quality.

Operating Life

The operating lifetime is 10,000 hours or more at 5 mA (operating life with LM000106 or equivalent).

The inverter should meet the following conditions:

- Sine, symmetric waveform without spike in positive and negative.
- The voltage at the secondary side is 1,000 V_{RMS} or more.
- Illuminance frequency is from 25 kHz to 45 kHz.

The operating lifetime is defined as having ended when any of the following conditions occur (25 ±5°C):

- When the voltage required for initial discharge has reached 900 V_{RMS} or when it has reached 10.8 V DC when used as an inverter.
- When the illuminence or quantity of light has decreased to 50% of the initial value.

NOTE: Ratings are defined as the average brightness inside the viewing area specified in Figure 12.

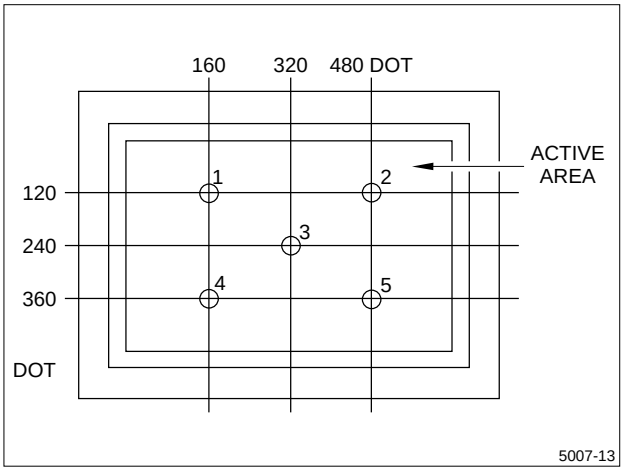


Figure 12. Measuring Points (1 to 5)

PRECAUTIONS

- Industrial (Mechanical) design of the product in which this LCD unit is incorporated must be so made that the viewing angle characteristics of the LCD are optimized. This unit's viewing angle is illustrated in Figure 13 and as follows:
  - θy MIN < viewing angle < θy MAX
    (θy MIN < 0°, θy MAX ≥ 0°)
    (For the specific values of θy MIN, θy MAX, refer to the Optical Characteristics Table.) Consider the optimum viewing conditions according to the purpose when installing the unit.

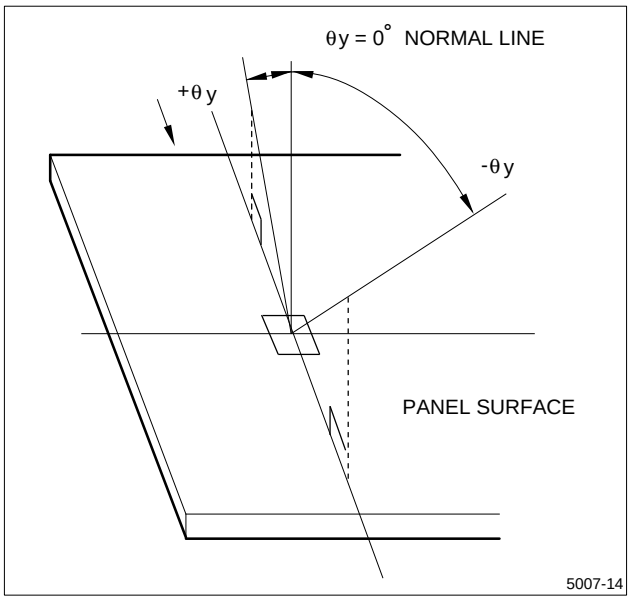
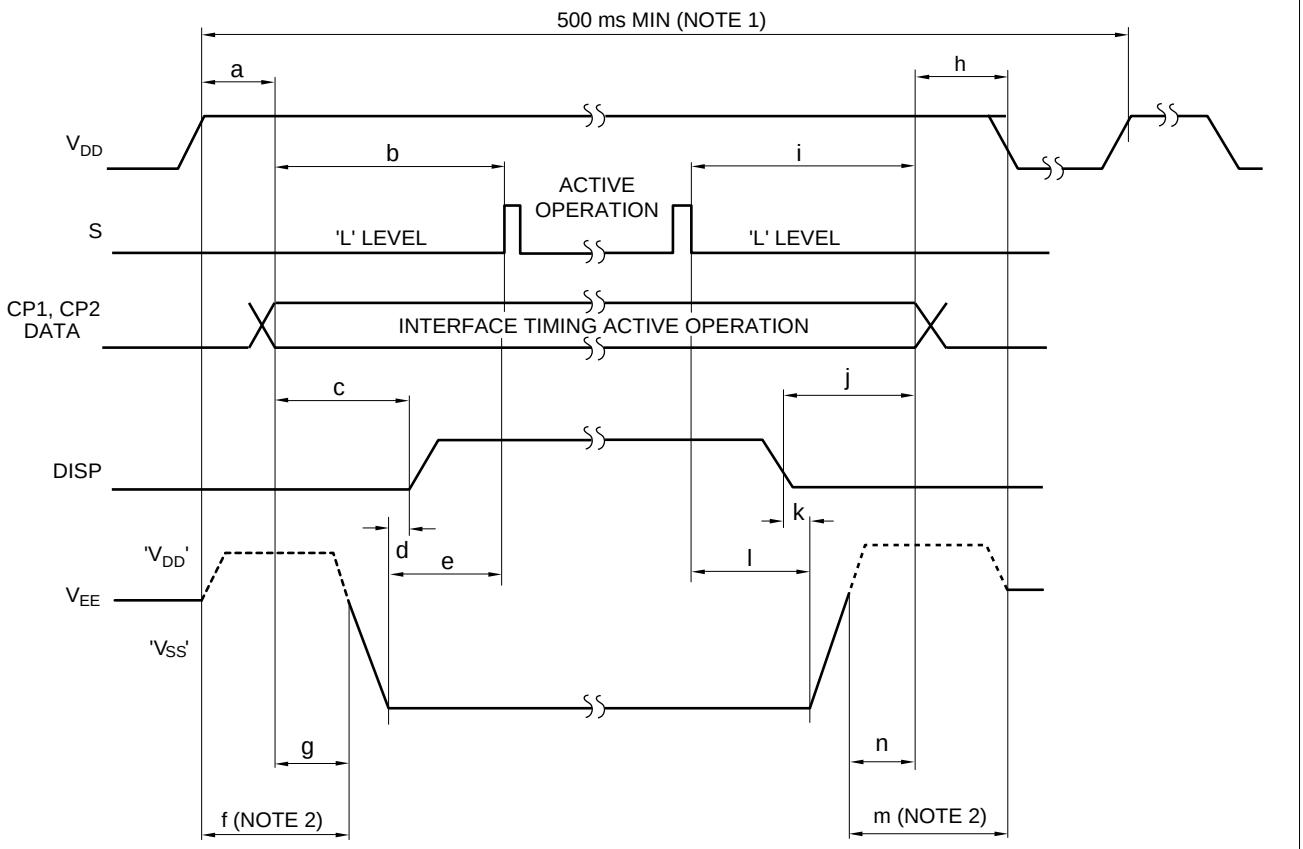


Figure 13. Dot Matrix LCD Viewing Angle

- This unit is installed using mounting tabs at the four corners of PCB or bezel. During installation, avoid undue stress on the unit such as twisting or bending. A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.
- Since the front polarizer is easily damaged, use care to not scratch the face.
- If the surface of the LCD cells need cleaning, wipe them with a soft cloth.
- Wipe liquid off immediately since it can cause color changes and staining.
- The LCD is made of glass plates. Use care when handling it to avoid breakage.
- This unit contains CMOS LSIs which are sensitive to electrostatic charges. The following measures should be taken to protect the unit from electrostatic discharge:
  - Ground the metallic case of the main system (contact of the unit and main system).
  - Insulate the unit and main system by attaching insulating washers made of bakelite or nylon.
- The unit should be driven according to the specified ratings to avoid malfunction or permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Avoid latch-up of driver LSIs and application of DC voltage to the LCD panel by following the ON/OFF sequence shown in Figure 14 and Table 1.
- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- Do not disassemble the unit.



NOTES:

1. Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.
2. V_{EE} to be set at 'V_{DD} level' or 'open.' V_{EE} should be in accordance with the dotted line when DISP (display control signal) is not used.

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Figure 14. Supply Voltage Sequence Condition

Table 1. Supply Voltage Sequence Condition

SYMBOL	WITH DISP CONTROL [1]	WITHOUT DISP CONTROL [2]
POWER ON		
a	0 ms (minimum)	0 ms (minimum) 20 ms (maximum)
b	0 ms (minimum)	20 ms (minimum)
c	20 ms (minimum)	–
d	0 ms (minimum)	–
e	–	0 ms (minimum)
f	0 ms (minimum)	Note 3
g	–	0 ms (minimum) 100 ms (maximum)
POWER OFF		
h	0 ms (minimum)	0 ms (minimum) 20 ms (maximum)
i	0 ms (minimum)	20 ms (minimum)
j	20 ms (minimum)	–
k	0 ms (minimum)	–
l	–	0 ms (minimum)
m	0 ms (minimum)	Note 3
n	–	100 ms (minimum)

NOTES:

1. Connection of DISP (pin number 4), refer to Figure 15.
2. Connection of DISP (pin number 4), refer to Figure 16.
3. V_{EE} to be set at 'V_{DD} level' or 'open.' V_{EE} should be in accordance with the dotted line when DISP (display control signal) is not used.

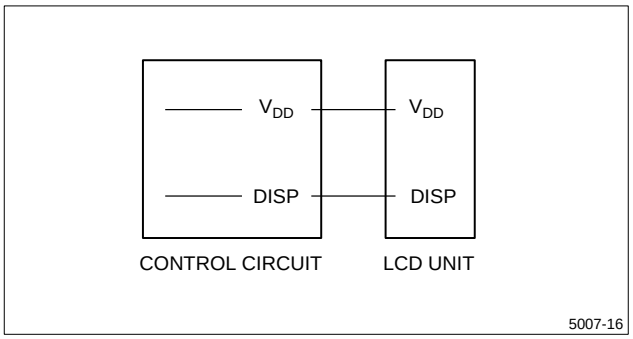


Figure 15. Connection With DISP Control Input DISP Control Signal Shown in Figure 14.

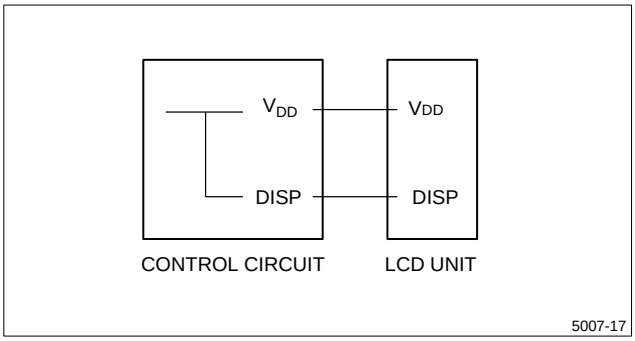


Figure 16. Connection Without DISP Control DISP to be Connected With V_{DD}

LOT NUMBER

Lot number is shown at the position mentioned in Figure 17 in accordance with the numbering rule shown in Figure 18.

APPLICABLE INSPECTION STANDARD

The LCD unit meets the following inspection standard: S-U-012-01.

DISPLAY QUALITY

This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, evaluate display quality for the usability of the LCD unit in case gray scale is displayed on the LCD unit.

WARNING: Don't use any materials which emit gas from epoxy resin (Amines' hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent polarizer color change caused by gas.

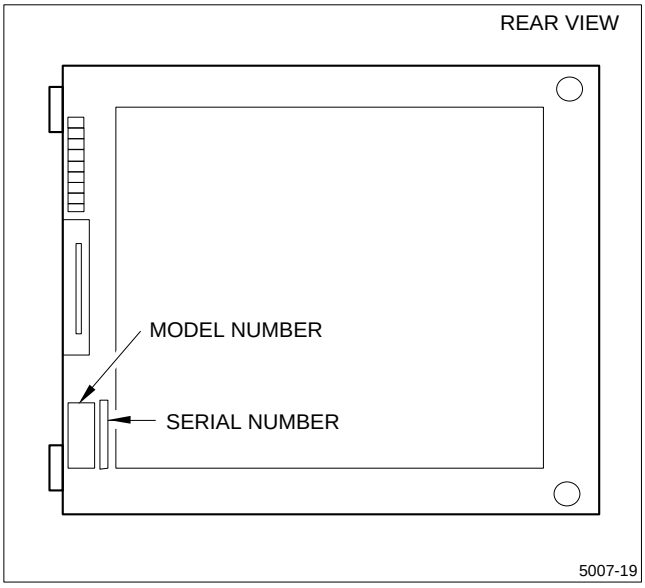


Figure 17. Lot Number Position

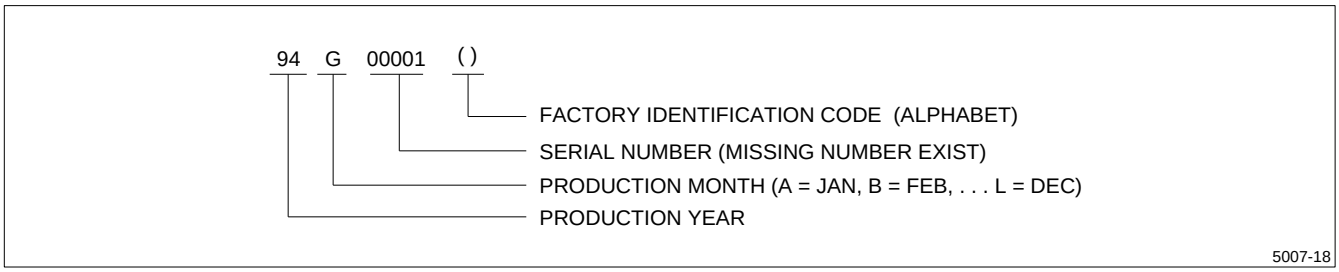
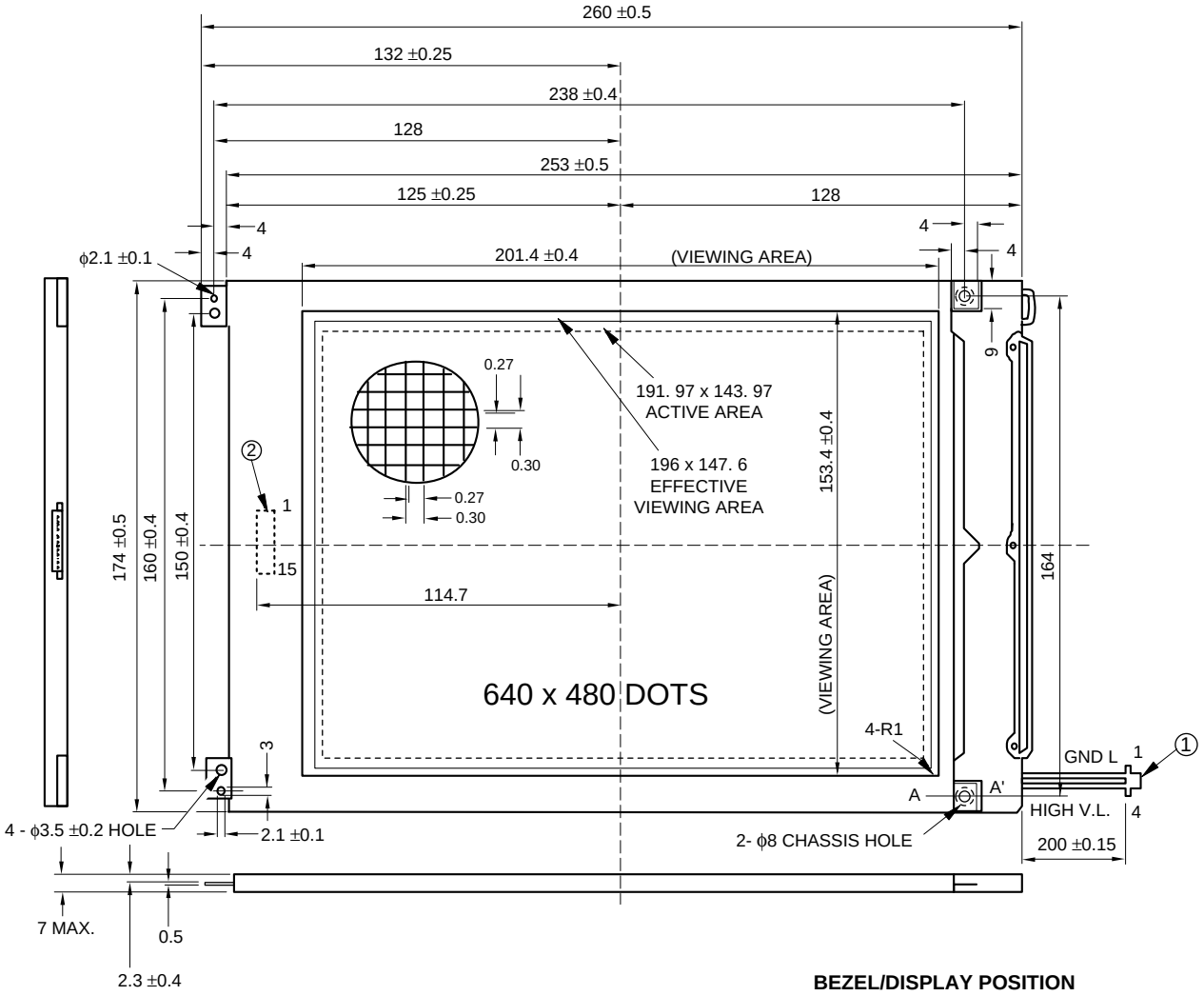
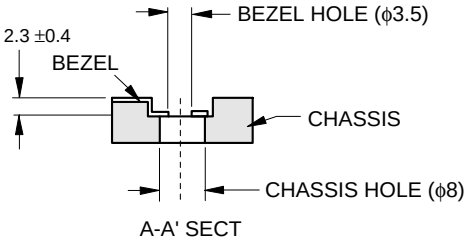


Figure 18. Numbering Rule

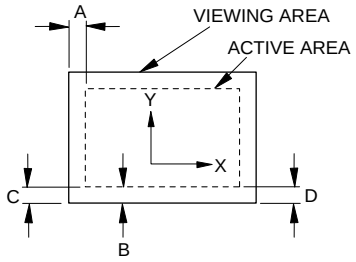
OUTLINE DIMENSIONS





A-A' SECT

BEZEL/DISPLAY POSITION



1. TOL (TOLERANCE) X-DIRECTION A: 4.7 ±0.8
2. TOL (TOLERANCE) Y-DIRECTION B: 4.7 ±0.8
3. OBLIQUITY OF DISPLAY AREA (C-D) <0.8

INTERFACE PIN LAYOUT

PIN #	1	2	3	4	5	6	7	8
SYMBOL	S	CP1	CP2	$DISP_{OFF}$	V_{DD}	V_{SS}	V_{EE}	DU_0
PIN #	9	10	11	12	13	14	15	
SYMBOL	DU_1	DU_2	DU_3	DL_0	DL_1	DL_2	DL_3	

① CCFT CONNECTOR
M63-M83-04 (MITSUMI)

② INTERFACE CONNECTOR (15 PINS)
53261-1510 (MOLEX)

5007-12